REMARKS

Claims 1-19 will be pending upon entry of the present amendment. Claims 1, 3, and 8 are amended, and claims 10-19 are newly submitted herewith.

The Examiner has rejected claims 1, 2, and 6 under 35 U.S.C. § 102(b) as being anticipated by Ngo et al. (U.S. Patent No. 6,127,261, hereafter "Ngo"). Claims 4 and 5 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Ngo, and claims 3 and 7-9 have been rejected under 35 U.S.C. § 103 as being unpatentable over Ngo in view of Dawson (U.S. Patent No. 5,503,882).

With respect to the rejections of claims 3 and 7-9, applicants note that the Examiner has cited a limitation that is not found in the original claims 3 or 7-9, stating, "However, Ngo et al. fail to teach forming a second layer... *directly overlying and being in contact with at least a portion of the borophosphorous silicate glass region having a planar surface.*" The Examiner then proceeds to cite Dawson, as teaching or suggesting this limitation.

While this limitation is not found in the original claims, the Examiner has anticipated, at least to a degree, amendments to claims 3 and 8. Accordingly, the applicants will address the Examiner's arguments, to the extent that they apply to the currently amended claims.

Prior to addressing the specific rejections, applicants wish to discuss particular aspects of the cited prior art.

Discussion of Prior Art

Ngo's FIG. 1 is reproduced as follows:

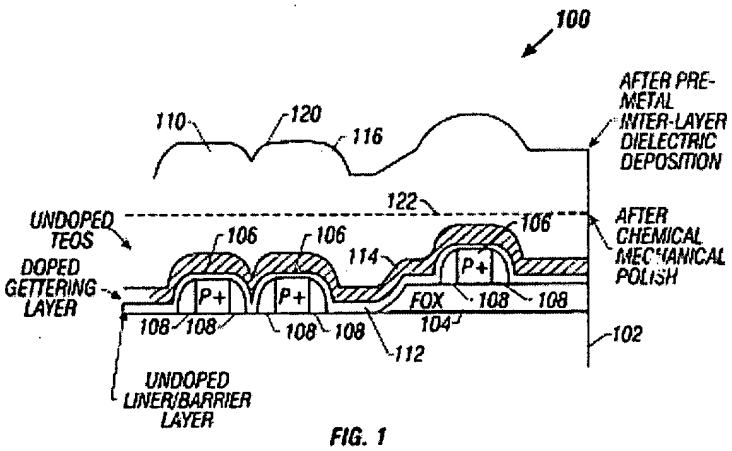

FIG. 1

With respect to FIG. 1, the text of Ngo states:

> Referring to FIG. 1, a cross-sectional view of an integrated circuit 100 shows an example of a trilayer premetal interlayer dielectric deposition. The integrated circuit 100 includes a silicon substrate 102. A field oxide region 104 is formed on one side of the substrate 102 and is used to isolate devices within the substrate 102. A plurality of polysilicon gates 106 are formed overlying the substrate 102. The polysilicon gates 106 have oxide spacers 108 for implantation of structures such as lightly-doped drain (LDD) structures. A tri-layer premetal dielectric 110 overlies the surface of the substrate 102. The three layers of the tri-layer premetal dielectric 110 include an undoped liner/barrier layer 112, a doped gettering layer 114 and an undoped TEOS layer 116. A solid line 120 shows the surface of the integrated circuit 100 overlying the tri-layer premetal dielectric 110 after deposition of the tri-layer but before any etching or polishing. *A dotted line 122 shows the surface of the integrated circuit 100 overlying the tri-layer premetal dielectric 110 after chemical mechanical polishing.*

Column 2, lines 31-49, emphasis added.

> The undoped TEOS layer 116 is utilized to fill any voids in the surface of the doped gettering layer 114. The undoped TEOS layer 116 fills voids caused by structures such as the polysilicon gates 106 and the field oxide region 104. The undoped TEOS layer 116 also adds thickness to the surface of the integrated circuit *so that all structures, even prominent structures overlying both the field oxide region 104 and the polysilicon gate 106 [are covered]*. The undoped TEOS layer 116 has a thickness of approximately 10200 angstroms. The total thickness of the trilayer premetal dielectric 110 is approximately 13700 angstroms with a standard deviation of approximately 200 angstroms and a final thickness after polishing of about 4000 angstroms.

Column 2, line 65- column 3, line 10, emphasis added.

The sentence quoted above is missing the verb and applicants have placed the words "are covered" at the end because it is believed this is what was intended by the inventor and corresponds to what is shown in the figure. Further support of this understanding may be found in Ngo's independent claims 1, 2, 14, 19, and 22. A polishing step is recited in every independent claim, including the limitation "without exposing the doped layer." (see column 5, lines 35 and 65, column 7, line 44, and column 8, lines 15 and 42.) Ngo clearly regards this limitation as being essential.

From Ngo's figures, specification, and claims a teaching is quite clear: Figure 1 shows the surface of the circuit after polishing at the dotted line 122, well above the upper

surface of the doped gettering layer 114, such that the doped gettering layer is not exposed; the specification states that "*...all structures, even prominent structures overlying both the field oxide region 104 and the polysilicon gate 106 [are covered]*"; and the claims, without exception, recite polishing the oxide layer *without exposing the doped layer.* Ngo clearly teaches away from exposing any of the underlying layers in the planarizing step.

Dawson's Figures 6b and 7b are reproduced herebelow. For clarity, applicants have inserted reference numeral 44, which is clearly shown in Figure 5, into Figure 6B.

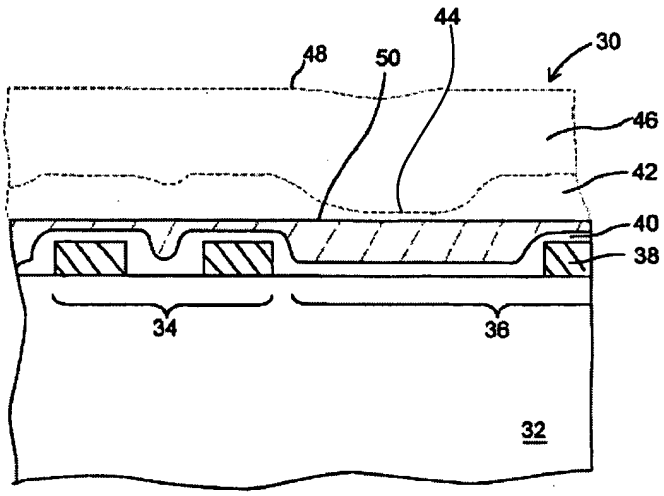

Fig. 6b

With respect to the structure shown in Figure 6B, Dawson states the following:

> It is important, however, that for reasons described below, the lowest elevational point for upper surface 44 [of TEOS oxide layer 42] *is above any and all plasma oxide 40.* A thicker TEOS oxide provides such elevational assurances.

Column 7, lines 43-46, emphasis added.

> Etch-back upper surface 50 is at approximately the same elevational level as the lowest elevation level of TEOS oxide 42 upper surface [44]. By maintaining TEOS oxide 42 upper surface within an area 36 above TEOS oxide 42 lower surface with an area 34, *etch-back upper surface 50 is assured of having a defined thickness of TEOS oxide 42 remaining across the entire wafer surface.*

Column 8, lines 54-61, emphasis added.

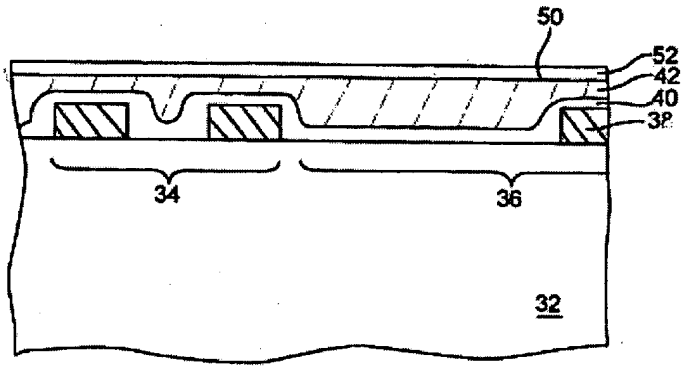

Fig. 7b

With respect to FIG. 7b, the text of Dawson states:

> Alternatively, capping layer 52 can be placed upon an etch-back upper surface 50 of FIG. 6b, as shown in FIG. 7b. Capping layer 52, in either embodiments of FIG. 7a or 7b, provide the advantages described above. Capping layer 52 upon etch-back upper surface 50, shown in FIG. 7b, ensures that the lower density TEOS oxide will not absorb moisture from an outside ambient. Capping layer 52 provides a barrier against absorption similar to the barrier formed above SOG layer 46, as shown in FIG. 7a.

Dawson Patent, col. 9 lines 20-30.

Figure 6B shows Dawson's device with an oxide layer 42 thickly deposited to upper surface 44, then etched back to etch-back surface 50. Dawson's text describes the importance of depositing the oxide layer 42 to a thickness sufficient that the lowest point of the upper surface 44 is above the highest point of the plasma oxide layer 40. In this way, when the oxide layer 42 is etched back to a planar surface 50, the layer is "assured of having a defined thickness of TEOS oxide 42 remaining across the entire wafer surface." Clearly, it is critical to Dawson that no portion of any underlying layers be exposed by the etch-back process.

Dawson's Figure 7B shows that the capping layer 52, deposited on the upper surface 50 of the oxide layer 42, does not make contact with any other layer or feature. In view of the text quoted, with reference to Figure 6B, there is no suggestion or teaching that the capping layer make contact with any layer beneath the oxide layer, but rather, a strong teaching away from such a structure.

Responsive Arguments

Amended claim 1 recites, in part, "planarizing the PE-TEOS layer such that a portion of the BPSG layer is exposed, to form a pre-metal dielectric stack." As was demonstrated previously in the discussion directed to the Ngo reference, Ngo clearly teaches away from planarizing a dielectric layer to the extent that any portion of an underlying layer is exposed, teaching, instead, the importance of providing sufficient thickness that even the most prominent structures are covered. Accordingly, claim 1 is allowable over the cited prior art. Dependent claims 2-9 are also therefore allowable.

While claims 3 and 8 are allowable as depending from an allowable base claim, applicants are of the opinion that claims 3 and 8 are allowable on their own merits as well. In rejecting these claims, the Examiner has cited the Ngo reference as teaching all of the limitations of base claim 1, while citing Dawson as teaching the respective limitations of claims 3 and 8. Amended claims 3 and 8 recite the steps of forming a TEOS layer and a PE-TEOS layer, respectively, on the planarized PE-TEOS layer *and contacting the portion of the BPSG layer*. As was shown in the discussion of the rejection of claim 1, above, Ngo fails to teach or suggest the limitation of planarizing the PE-TEOS layer such that a portion of the BPSG layer is exposed. In view of the discussion of the Dawson reference, above, it is clear that Dawson cannot provide this missing teaching. Furthermore, because Dawson teaches away from exposing any of the underlying structure during the etch-back step, Dawson cannot provide a teaching or suggestion of forming a further layer contacting a portion of the BPSG layer. Accordingly, claims 3 and 8 are allowable over the cited prior art.

In view of the allowability of base claim 1, the remaining rejections are moot.

New claims 10-19 have been submitted to capture previously unclaimed scope enabled by the specification. In particular, it is clear, based upon a reading of pages 1, 2, and 4 of the specification, that the invention is not limited to the particular composition of layers recited in claim 1. Accordingly, new claims 10-19 are submitted to more broadly claim the invention. Nevertheless, independent claim 10 recites, in part, "planarizing the third layer to a degree that a portion of the second layer is exposed." As has been previously demonstrated, both the cited references teach away from such a process step. Accordingly, claim 10, together with dependent claims 11-19, is allowable over the cited prior art.

Drawings - Figures 1-6 have been amended to correct a typographical error. Two sheets of drawings are presented herewith for approval.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicants' undersigned representative at (206) 622-4900 in order to expeditiously resolve prosecution of this application.

The Commissioner is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

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HHB:wt
Enclosures:
Postcard
2 Sheets of Replacement Drawings (Figures. 1-6)

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